Fig.1

PRIOR ART

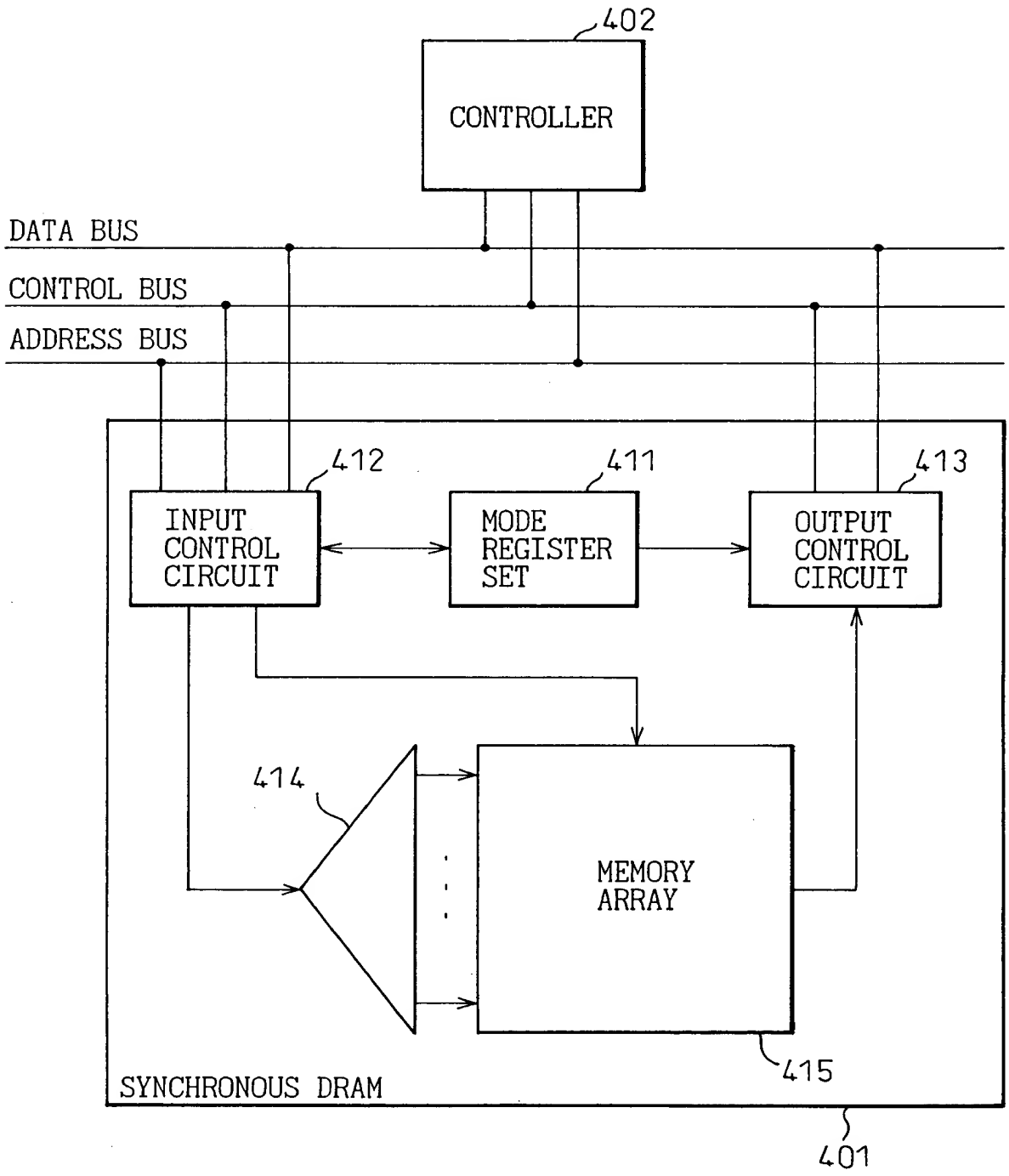

Fig.2

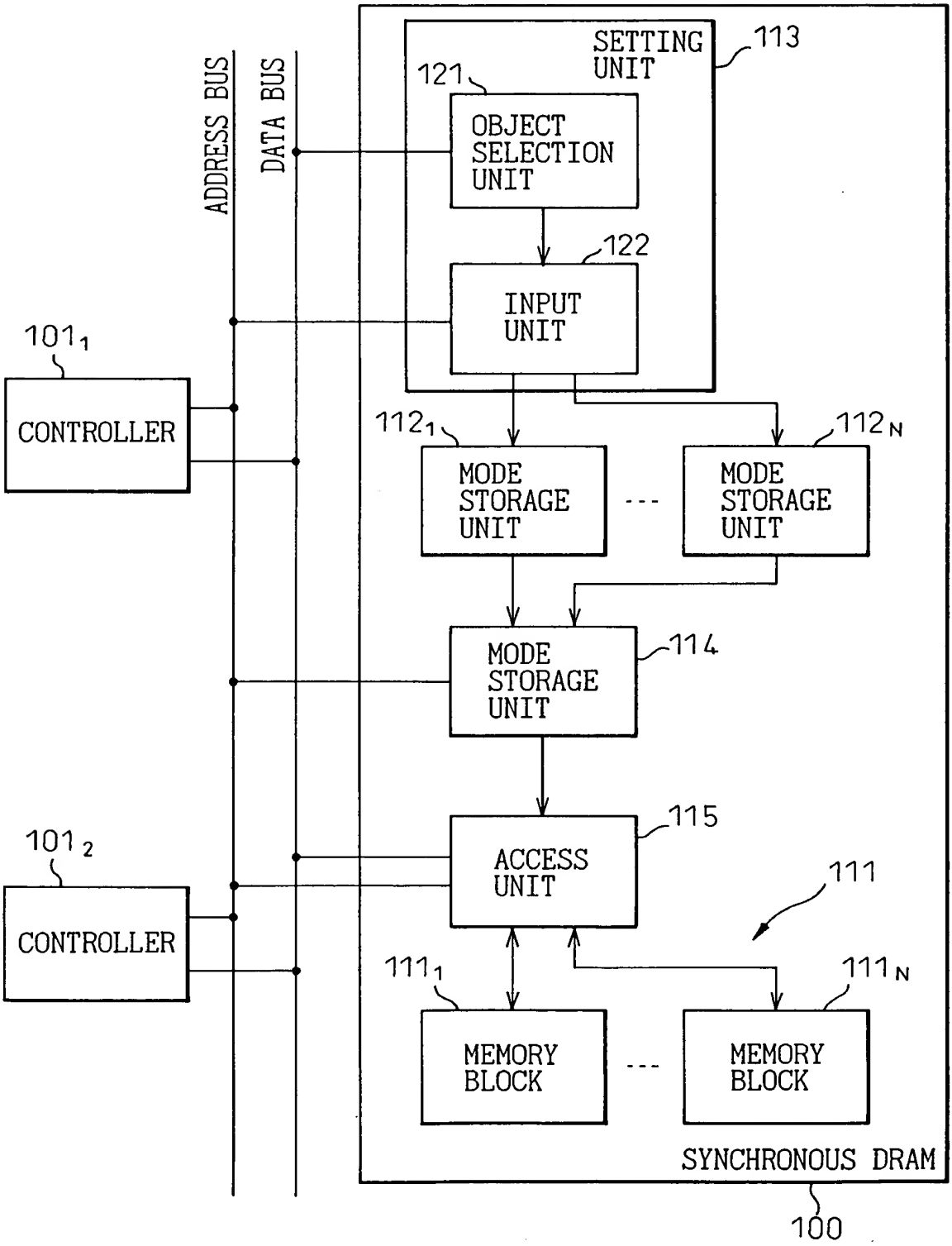
SETTING UNIT
113
121
OBJECT SELECTION UNIT
122
INPUT UNIT
ADDRESS BUS
DATA BUS
101 1
CONTROLLER
112 1
MODE STORAGE UNIT
112 N
MODE STORAGE UNIT
MODE STORAGE UNIT
114
101 2
CONTROLLER
115
ACCESS UNIT
111
111 1
MEMORY BLOCK
111 N
MEMORY BLOCK
SYNCHRONOUS DRAM
100

Fig.3

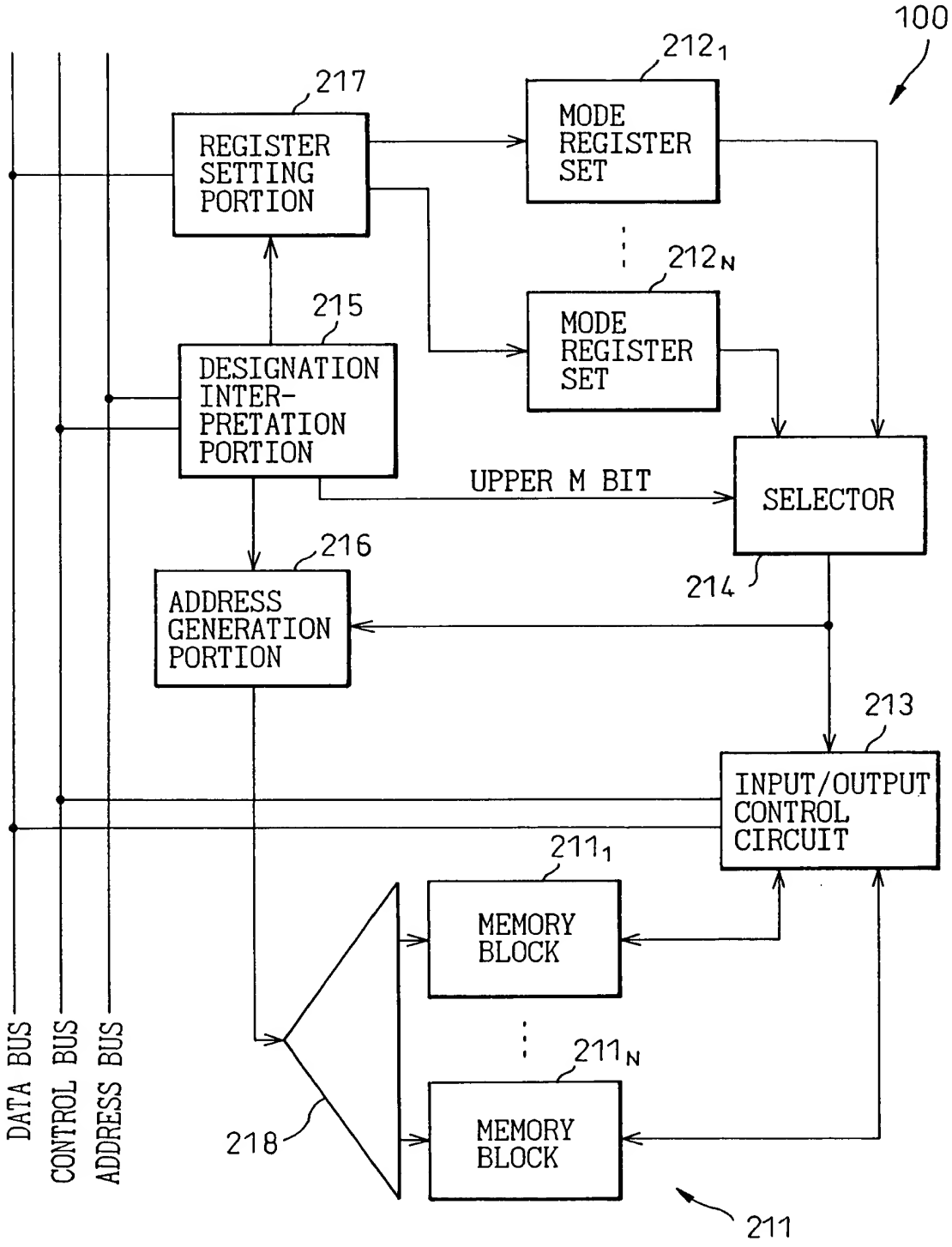
100
212_1
217
REGISTER SETTING PORTION
MODE REGISTER SET
212_N
215
MODE REGISTER SET
DESIGNATION INTER-PRETATION PORTION
UPPER M BIT
SELECTOR
216
214
ADDRESS GENERATION PORTION
213
INPUT/OUTPUT CONTROL CIRCUIT
211_1
MEMORY BLOCK
211_N
MEMORY BLOCK
218
DATA BUS
CONTROL BUS
ADDRESS BUS
211

Fig.4

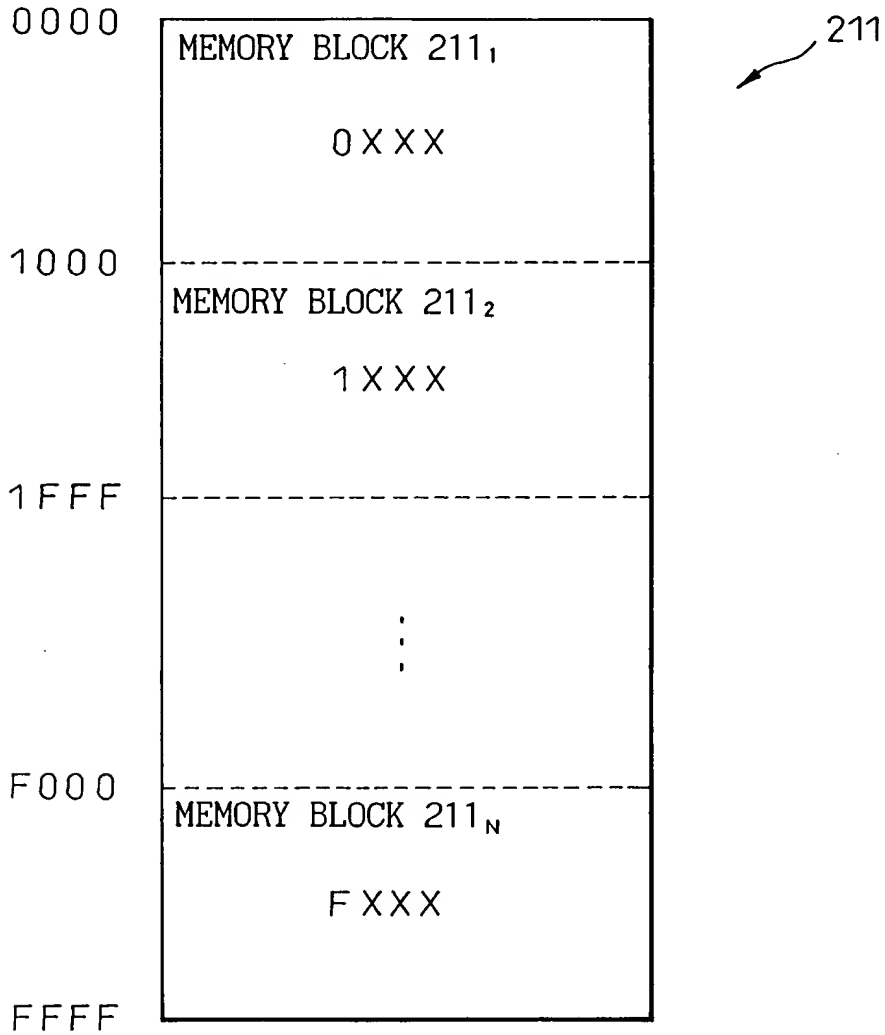
0000
1000
1FFF
F000
FFFF
MEMORY BLOCK 211₁
0XXX
MEMORY BLOCK 211₂
1XXX
MEMORY BLOCK 211N
FXXX
211

Fig.5A

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
WBL	TEST MODE		CAS LATENCY			BT	BURST LENGTH		

WBL: WRITE BURST LENGTH
BT: BURST TYPE

Fig.5D

TEST MODE

A8	A7	
0	0	OPERATION MODE SETTING
0	1	SPARE
1	0	SPARE
1	1	SPARE

Fig.5C

CAS LATENCY

A6	A5	A4	
0	0	0	SPARE
0	0	1	2
0	1	0	3
0	1	1	SPARE
⋮	⋮	⋮	⋮
1	1	1	SPARE

Fig.5B

BUST LENGTH

A2	A1	A0	BT = 0	BT = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	SPARE	SPARE
⋮	⋮	⋮	⋮	⋮
1	1	1	FULL BURST	SPARE

Fig.5E

A9	WBL
0	BURST
1	SINGLE BIT
A3	BT
0	SEQUENTIAL
1	INTERLEAVE

Fig.6A

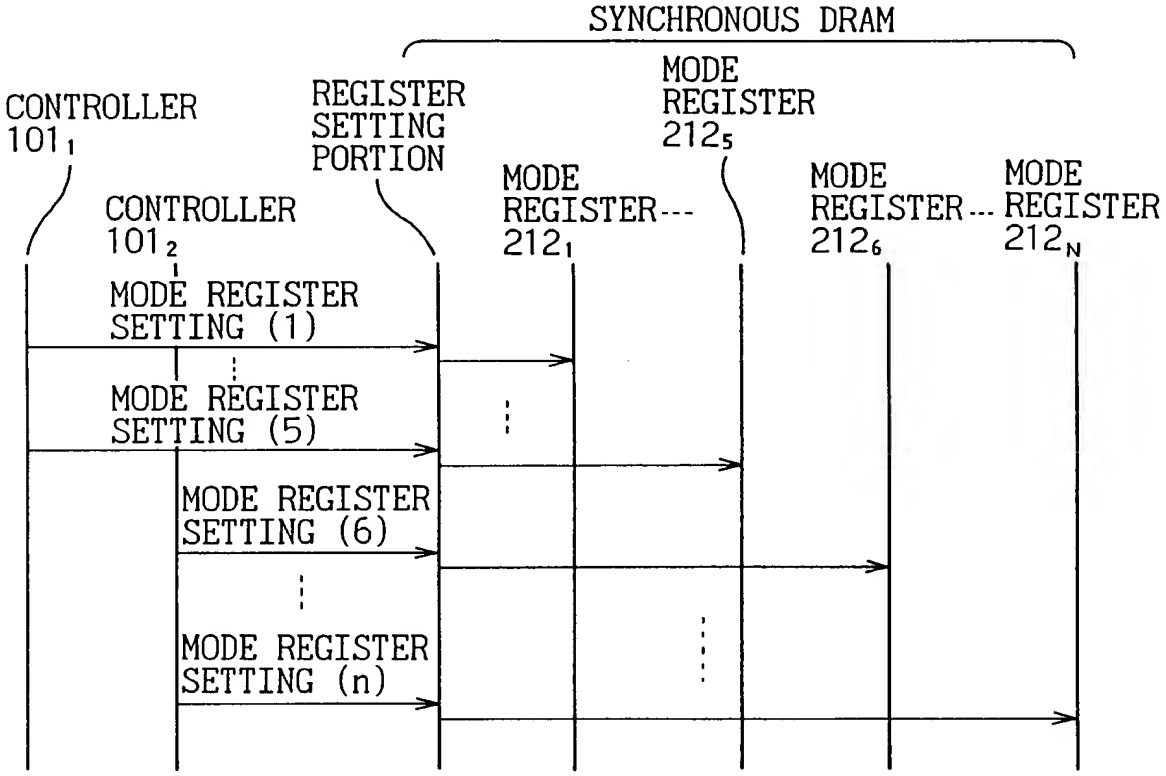
SYNCHRONOUS DRAM
CONTROLLER 101₁
CONTROLLER 101₂
REGISTER SETTING PORTION
MODE REGISTER 212₅
MODE REGISTER 212₁
MODE REGISTER 212₆
MODE REGISTER 212N
MODE REGISTER SETTING (1)
MODE REGISTER SETTING (5)
MODE REGISTER SETTING (6)
MODE REGISTER SETTING (n)

Fig.6B

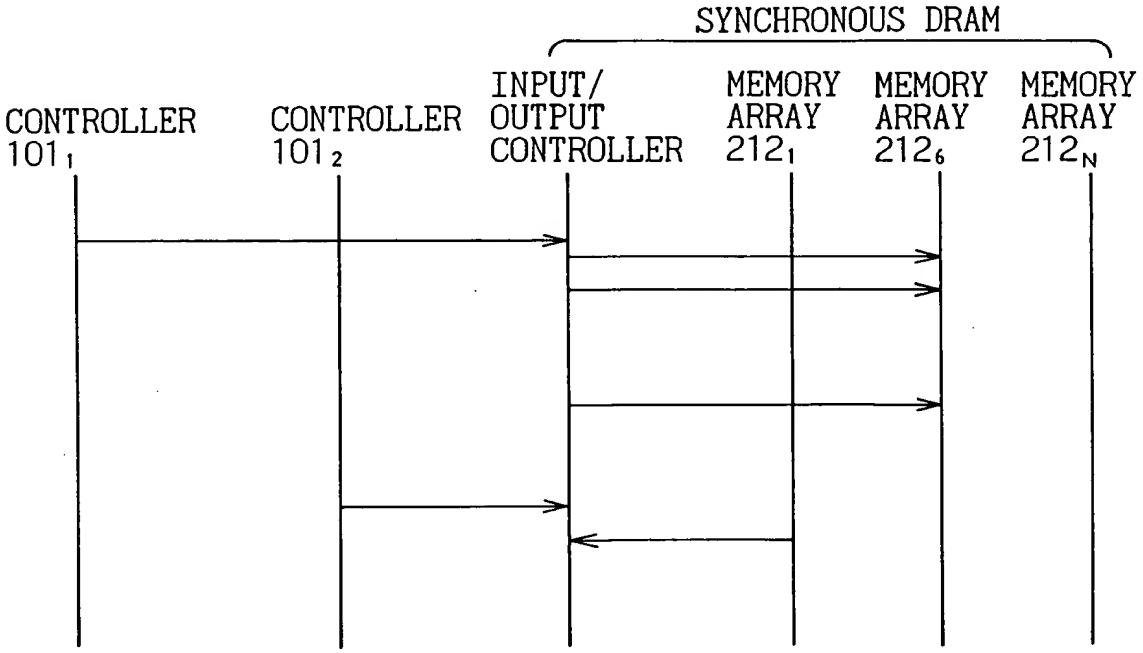
SYNCHRONOUS DRAM
CONTROLLER 101₁
CONTROLLER 101₂
INPUT/ OUTPUT CONTROLLER
MEMORY ARRAY 212₁
MEMORY ARRAY 212₆
MEMORY ARRAY 212N

Fig.7

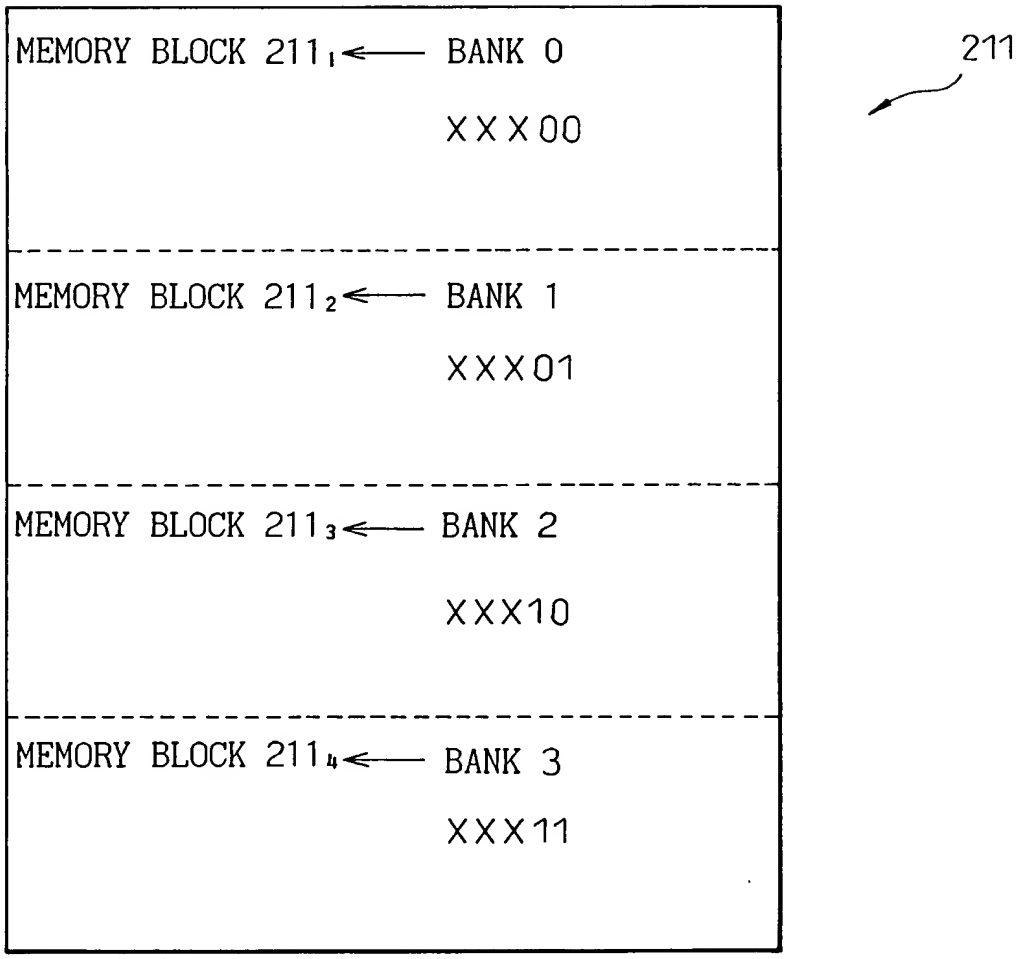
MEMORY BLOCK 211₁ ← BANK 0
XXX00
MEMORY BLOCK 211₂ ← BANK 1
XXX01
MEMORY BLOCK 211₃ ← BANK 2
XXX10
MEMORY BLOCK 211₄ ← BANK 3
XXX11
211

Fig.8

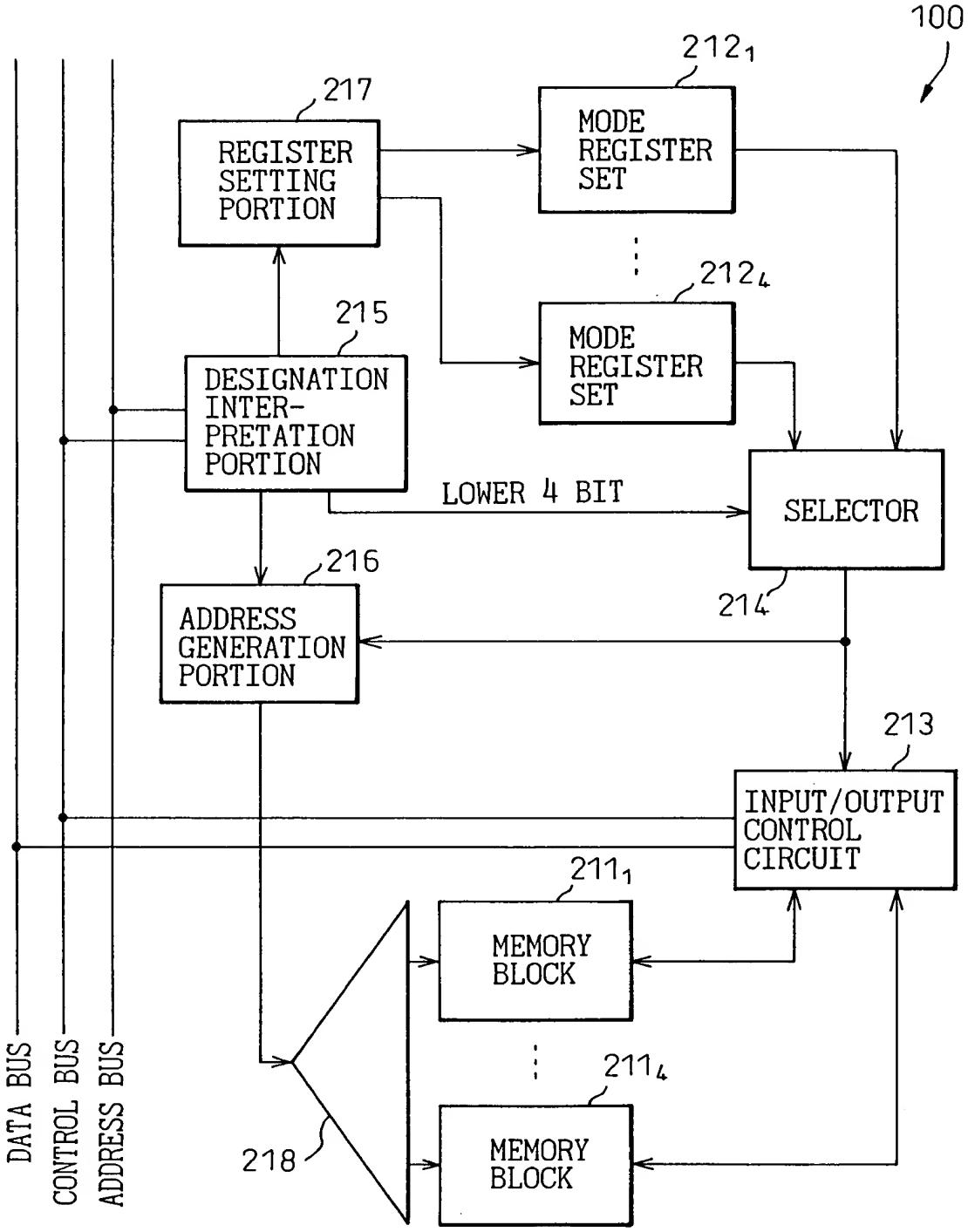
100
212_1
217
REGISTER SETTING PORTION
MODE REGISTER SET
212_4
215
MODE REGISTER SET
DESIGNATION INTER-PRETATION PORTION
LOWER 4 BIT
SELECTOR
216
214
ADDRESS GENERATION PORTION
213
INPUT/OUTPUT CONTROL CIRCUIT
211_1
MEMORY BLOCK
211_4
MEMORY BLOCK
218
DATA BUS
CONTROL BUS
ADDRESS BUS

Fig.9

A9	A8	A7	A6	A5	A4	A3	A2	A1	A0
WBL	TEST MODE		CAS LATENCY			BT	BURST LENGTH		

WBL: WRITE BURST LENGTH
BT: BURST TYPE

TEST MODE

A8	A7	
0	0	OPERATION MODE SETTING (1)
0	1	OPERATION MODE SETTING (2)
1	0	OPERATION MODE SETTING (3)
1	1	OPERATION MODE SETTING (4)